MSc Thesis Project
Error-Correction for 1 Tbit/s Optical Communication and its FPGA implementation

Introduction: DTU Fotonik has suggested product codes as error-correcting codes for very high speed optical communication, and a single FPGA has been implemented for 1600 Gbit/s. Product codes are constructed as two-dimensional arrays where each row and column belongs to some component code. Iterative decoding is employed as decoding method with great decoding performance. The code implemented has an overhead of 6.7% and is able to reduce the bit error rate below $10^{-15}$. However it is believed that the error rate on the optical fiber connection may be higher than what was designed for (around $4 \cdot 10^{-3}$), so a stronger error-correcting code is needed.

Contents: The performance may be better, if the component codes could correct four or more errors instead of the three errors in the present implementation. The first task of this project is to study suitable architectures for a component decoder capable of correcting four errors. Implementation of such a decoder in VHDL and integration into a complete system for at least 1 Tbit/s could follow next. Dependent on the interest of the student, architectures for correction of five errors in the component codes could also be investigated.

Prerequisites:
- 01405 Error-Correcting codes (or 34220 with a little extra effort)
- 34251 Convolutional codes and iterative decoding methods
- Knowledge of VHDL coding techniques, e.g. from 34349 FPGA design for Communication systems

Additional information:
- I.B. Djordjevic, "Advanced Coding for Optical Communications", Chapter 6 of "I.P. Kaminov (Ed.): Optical Fiber Telecommunication Communication VIB"
- Okano & Imai, "A Construction Method of High-Speed Decoders Using ROM’s for Bose-Chaudhuri-Hocquenghem and Reed-Solomon Codes"
- Contact teacher.

Practical details: The project is intended for 1 or 2 students with 30 ECTS-points per student.

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